REMARKS

This is in response to the Office Action mailed on March 15, 2004, and the references cited therewith.

Claims 1, 4, 8, 10-13 and 21-27 are amended, and claims 28-29 are canceled herein. As a result, claims 1, 4, 8, 10-13 and 21-27 are now pending in this application. Claims 1, 4, 8, 10-13 and 21-27 were not amended in response to an art rejection, but were amended to clarify the meaning of a term in the claims. The amendments are not intended to limit the scope of equivalents to which any claim element may be entitled. The amendments to the claims are fully supported by the specification as originally filed, and no new matter has been added.

The Office Action Summary at Checkbox 4 states that "Claim(s) 1, 4, 8, 10-13, and 22-29 is/are pending in the application." Applicant respectfully submits that claim 21 is also still pending in the application. The Office Action Summary at Checkbox 6 states, "Claim(s) 1, 4, 8, 10-13, and 22-29 is/are rejected." Further, on page 2 the Office Action states, "Claims 1, 4, 8, 10-13 and 22-29 are rejected under 35 U.S.C. 112," but then goes on to describe a basis for a rejection of claim 21. However, on page 3 the Office Action states, "Claims 1, 4, 8, 10-13 and 21-19 would be allowed if rewritten to overcome the rejection(s) under 35 U.S.C. 112." (Emphasis added.) Because the Applicant submits that claim 21 is still pending in the application, the Applicant has proceeded, without admitting, that claim 21 was rejected by the examiner. The Applicant requests confirmation of the status of claim 21 in the next official action.

§112 Rejection of the Claims

Claims 1, 4, 8, 10-13 and 22-29 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claims 1, 4, 8, 10-13 and 22-27 have been amended to more particularly point out and distinctly claim the subject matter. In particular the physical structure of the logic components is now claimed rather than the function of the logic circuit. The Applicant

submits that the objections to claims 1, 4, 8, 10-13 and 22-27 under 35 USC 112 are now overcome and the claims are in condition for allowance. However, in further support of the claims, the Application also submits the following remarks.

The objection to lines 8-11 of claim 1 appears to be based on the fact that the word "or" has been omitted prior to the words "AND logic for combining". Thus, there are only two possible types of elementary OR symmetric function logic defined in the claim, and only two possible types of elementary EXOR symmetric function logic defined in the claim.

However, the Applicant wishes to clarify the claim to explicitly include a third option, i.e. that AND logic is also a type of elementary OR or EXOR symmetric function logic, in the case where the set size k is equal to the total number of inputs. If the set size k is equal to the total number of inputs, then there is only one possible set. Therefore, there is no need for OR or EXOR logic with its input connected to the output of a single AND gate, because the final output will always take the same value as the output of the AND gate. An example is the OR_3_3, which is shown in figure 13.

In lines 10 and 12 of claim 1, the definitions of m and k have been moved to occur earlier in the claim.

In lines 15-18 of claim 1, the EXOR_5_3 is not simply the EXOR gate of figure 9, but the entire circuit of figure 9, i.e. the AND/EXOR combination. The inputs are X1 to X5, which are parallel counter inputs (see page 9, line 18), and the output of figure 9 is a binary output of the type shown in figure 3. It appears that the Office Action does not take into account that the EXOR_5_3 is the entire circuit of figure 9, rather than just the EXOR gate.

Claim 4 includes a positive recitation of one of the options of claim 1. Claims 4, 8, 11 and 13 have been re-worded to make it clear how the "logic to ..." relates to the elementary OR and EXOR symmetric function logic of claim 1.

Claims 10 and 12 have been amended to make it clear how they are adapted.

In claim 21, the "binary numbers" of line 1 have been amended to "first and second" binary numbers, and the "binary numbers" of line 7 have been amended to "binary numbers of the reduced array" to make the distinction between them clear.

Claims 21-27 have been amended in a similar manner to claims 1, 4, 8 and 10-13.

Claims 28 and 29 have now been canceled.

Reconsideration and withdrawal of the rejection under 35 USC 112 is respectfully requested in view of the above remarks.

Allowable Subject Matter

Claims 1, 4, 8, 10-13 and 21-29 were indicated to be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. § 112 set forth in the Office Action. Applicant believes that claims 1, 4, 8, 10-13 and 21-27, as amended, comply with the requirements of 35 U.S.C. § 112. Claims 28 and 29 are cancelled. Applicant accordingly requests allowance of claims 1, 4, 8, 10-13 and 21-27.

Double Patenting Rejection

The Examiner has rejected claims 1, 4, 8, 10-13 and 21-29 of this application as conflicting with claims 1-3, 16, 18-24, 26, 28, 30-33 and 41 of Application No. 09/769,954. Claims 28 and 29 are canceled, so rejection of claims 28 and 29 is moot. The Applicant respectfully traverses the rejection of claims 1, 4, 8, 10-13, and 21-27. The Office Action states:

> "37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822."

Since there is no mention of obviousness or of nonstatutory nature, Applicant will treat the rejection as a statutory provisional double patenting rejection. However, in doing so, Applicant is expressly not admitting that such a rejection is appropriate, and

will demonstrate that the rejection is improper. Furthermore, if the rejection was not intended by the Examiner to be a statutory provisional double patenting rejection, Applicant respectfully requests clarification and an opportunity to respond to the clarified rejection.

"In determining whether a statutory basis for a double patenting rejection exists, the question to be asked is: Is the same invention being claimed twice?...Same Invention means identical subject matter. *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1984); *In re Vogel*, 422 F.2d 438, 164 U.S.P.Q. 619 (C.C.P.A. 1970); and *In re Ockert*, 245, F.2d 467, 114 U.S.P.Q. 330 (C.C.P.A. 1957)." MPEP ' 804. The MPEP further states that "[a] reliable test for double patenting under 35 U.S.C. ' 101 is whether a claim in the application could be literally infringed without literally infringing a corresponding claim in the patent. *In re Vogel*, 422 F.2d 438, 164 U.S.P.Q. 619 (C.C.P.A. 1970). Is there an embodiment of the invention that falls within the scope of one claim, but not the other? If there is such an embodiment, then identical subject matter is not defined by both claims and statutory double patenting would not exist."

The Applicant submits that there is no conflict between this application and application no. 09/769,954, because this application is concerned with generation of elementary symmetric function outputs using certain specific types of logic circuit, but application no. 09/769,954 is concerned with generation of a middle output of a parallel counter, using combinations of subcircuit outputs. These combinations of subcircuit outputs do not correspond to the circuits defined in the claims of the present application.

Claim 1 of the 09/769,954 application recites, "each EXOR logic unit is arranged to generate logic unit binary outputs," which is not recited in any of the pending claims of this application. Thus, a device which literally infringes the claims of this application may not have the elements needed for literal infringement of claim 1 of the 09/769,954 application. Thus, identical subject matter is not defined by this application and claim 1 of the 09/769,954 application. Therefore, a statutory double patenting rejection based on claim 1 of the 09/769,954 application in regards to all pending claims in this application is inappropriate.

Claims 2 and 3 of the 09/769,954 application depend on claim 1 and therefore contain all the elements and limitations of claim 1. For reasons analogous to those stated above with regards to claim 1 of the 09/769,954 application, a statutory double patenting rejection based on claims 2 and 3 of the 09/769,954 application is inappropriate.

Claim 16 of the 09/769,954 application recites, "each EXOR logic unit includes logic to generate logic unit binary outputs," which is not recited in any of the pending claims of this application. For reasons analogous to those stated above with regards to claim 1 of the 09/769,954 application, a statutory double patenting rejection based on claim 16 of the 09/769,954 application is inappropriate.

Claims 18 and 19 the 09/769,954 application recite "a conditional parallel counter having m possible high inputs out of n input," which is not recited in any of the pending claims of this application. For reasons analogous to those stated above with regards to claim 1 of the 09/769,954 application, a statutory double patenting rejection based on claims 18 and 19 of the 09/769,954 application is inappropriate.

Claim 20 of the 09/769,954 application recites "a digital filter," which is not recited in any of the pending claims of this application. For reasons analogous to those stated above with regards to claim 1 of the 09/769,954 application, a statutory double patenting rejection based on claim 20 of the 09/769,954 application is inappropriate.

Claim 21 of the 09/769,954 application recites, "logic circuit connected between the inputs and the outputs and for generating at least two of the plurality of binary outputs as elementary EXOR symmetric function functions of the binary inputs," which is not recited in any of the pending claims of this application. For reasons analogous to those stated above with regards to claim 1 of the 09/769,954 application, a statutory double patenting rejection based on claim 21 of the 09/769,954 application is inappropriate.

Claims 22-24, 26, 28, and 30-33 of the 09/769,954 application depend on claim 21 and therefore contain all the elements and limitations of claim 21. For reasons analogous to those stated above with regards to claim 1 of the 09/769,954 application, a statutory double patenting rejection based on claims 22-24, 26, 28, and 30-33 of the 09/769,954 application is inappropriate.

Claim 41 of the 09/769,954 application is cancelled, so a rejection based on claim 41 of the 09/769,954 application is inappropriate.

Therefore, the statutory double patenting rejection is improper. Applicant respectfully requests removal of the rejection and allowance of claims 1, 4, 8, 10-13, and 21-27.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9592 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15th day of September, 2004.

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Name

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